LEVEL 1 - 1 OF 2 PATENTS

6,269,128

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July 31, 2001

Clock recovery control in differential detection

CORE TERMS: clock, width, corrective, phase, variance, symbol, differential, counter, detector, digital...

LEVEL 1 2 OF 2 PATENTS

5,867,542

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Feb. 2, 1999

Clock phase detecting circuit and clock regenerating circuit each arranged in receiving unit of multiplex radio equipment

CORE TERMS: clock, identification, conversion, phase, converter, inclination, detect, oscillating, orthogonal, input...

5,867,542 OR 5867542

LEXIS-NEXIS
Library: PATENT
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5,867,542 OR 5867542

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File: JNLS

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CHEMICAL BUSINESS NEWSBASE

February 1, 2000

LENGTH: 239 words

HEADLINE: PRESS RELEASE: Sotralentz buys European reconditioners

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... West Industrial Estate,Peterlee, Co Durham SR8 2HR, UK. Tel: 0191 586 0577. Fax: 0191 5867542.

1/39/1
DIALOG(R)File 345:Inpadoc/Fam.& Legal Stat

13196336
Basic Patent (No,Kind,Date): EP 732829 A2 19960918 <No. of Patents: 004>
Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date	
EP 732829	A2	19960918	EP 95118303	A	19951121	(BASIC)
EP 732829	A3	19990915	EP 95118303	A	19951121	
JP 8256188	A2	19961001	JP 9559377	A	19950317	
US 5867542	A	19990202	US 552543	A	19951103	

Priority Data (No,Kind,Date):
JP 9559377 A 19950317

PATENT FAMILY:
EUROPEAN PATENT OFFICE (EP)
Patent (No,Kind,Date): EP 732829 A2 19960918
CLOCK PHASE DETECTING CIRCUIT AND CLOCK REGENERATING CIRCUIT EACH ARRANGED IN RECEIVING UNIT OF MULTIPLEX RADIO EQUIPMENT Clock phase detecting circuit and clock regenerating circuit each arranged in receiving unit of multiplex radio equipment (English; French; German)
Patent Assignee: FUJITSU LTD (JP)
Author (Inventor): IWAMATSU TAKANORI (JP); KIYANAGI HIROYUKI (JP)
Priority (No,Kind,Date): JP 9559377 A 19950317
Applic (No,Kind,Date): EP 95118303 A 19951121
Designated States: (National) DE; GB; IT
IPC: * H04L-007/02
Derwent WPI Acc No: * G 96-414781; G 96-414781
Language of Document: English
Patent (No,Kind,Date): EP 732829 A3 19990915
CLOCK PHASE DETECTING CIRCUIT AND CLOCK REGENERATING CIRCUIT EACH ARRANGED IN RECEIVING UNIT OF MULTIPLEX RADIO EQUIPMENT (English; French; German)
Patent Assignee: FUJITSU LTD (JP)
Author (Inventor): IWAMATSU TAKANORI (JP); KIYANAGI HIROYUKI (JP)
Priority (No,Kind,Date): JP 9559377 A 19950317
Applic (No,Kind,Date): EP 95118303 A 19951121
Designated States: (National) DE; GB; IT
IPC: * H04L-007/02
Derwent WPI Acc No: * G 96-414781
Language of Document: English

EUROPEAN PATENT OFFICE (EP)
Legal Status (No,Type,Date,Code,Text):

EP 732829	P	19950317	EP AA	PRIORITY (PATENT APPLICATION) (PRIORITAET (PATENTANMELDUNG)) JP 9559377 A 19950317
EP 732829	P	19951121	EP AE	EP-APPLICATION (EUROPAEISCHE ANMELDUNG) EP 95118303 A 19951121
EP 732829	P	19960918	EP AK	DESIGNATED CONTRACTING STATES IN AN APPLICATION WITHOUT SEARCH REPORT: (IN EINER ANMELDUNG OHNE RECHERCHENBERICHT BENANNTE VERTRAGSSTAATEN) DE GB IT
EP 732829	P	19960918	EP A2	PUBLICATION OF APPLICATION WITHOUT SEARCH REPORT (VEROEFFENTLICHUNG DER ANMELDUNG OHNE RECHERCHENBERICHT)
EP 732829	P	19961127	EP RIN1	INVENTOR (CORRECTION) (ERFINDER (KORR.)) IWAMATSU, TAKANORI, C/O FUJITSU LIMITED ; KIYANAGI, HIROYUKI, C/O FUJITSU TOHOKU
EP 732829	P	19990915	EP AK	DESIGNATED CONTRACTING

STATES IN A SEARCH REPORT: [redacted]N EINEM RECHERCHENBERICHT BENANNTE VERTRAGSSTAATEN) DE GB IT

EP 732829 P 19990915 EP A3 SEPARATE PUBLICATION OF THE SEARCH REPORT (ART. 93) (GESONDERTE VEROEFFENTLICHUNG DES RECHERCHENBERICHTS (ART. 93))

EP 732829 P 19991103 EP 17P REQUEST FOR EXAMINATION FILED (PRUEFUNGSANTRAG GESTELLT) 19990906

JAPAN (JP)
Patent (No,Kind,Date): JP 8256188 A2 19961001
CLOCK PHASE DETECTION CIRCUIT AND CLOCK REPRODUCING CIRCUIT PROVIDED IN RECEPTION PART OF MULTIPLE RADIO EQUIPMENT (English)
Patent Assignee: FUJITSU LTD
Author (Inventor): IWAMATSU TAKANORI; ONIYANAGI HIROYUKI
Priority (No,Kind,Date): JP 9559377 A 19950317
Applic (No,Kind,Date): JP 9559377 A 19950317
IPC: * H04L-027/22; H04L-007/00; H04L-027/38
Derwent WPI Acc No: * G 96-414781
Language of Document: Japanese

UNITED STATES OF AMERICA (US)
Patent (No,Kind,Date): US 5867542 A 19990202
CLOCK PHASE DETECTING CIRCUIT AND CLOCK REGENERATING CIRCUIT EACH ARRANGED IN RECEIVING UNIT OF MULTIPLEX RADIO EQUIPMENT (English)
Patent Assignee: FUJITSU LTD (JP)
Author (Inventor): IWAMATSU TAKANORI (JP); KIYANAGI HIROYUKI (JP)
Priority (No,Kind,Date): JP 9559377 A 19950317
Applic (No,Kind,Date): US 552543 A 19951103
National Class: * 375354000; 375326000; 375332000; 375344000; 329304000
IPC: * H04L-007/02; H04L-027/22
Derwent WPI Acc No: * G 96-414781
Language of Document: English

UNITED STATES OF AMERICA (US)
Legal Status (No,Type,Date,Code,Text):
US 5867542 P 19950317 US AA PRIORITY (PATENT)
JP 9559377 A 19950317
US 5867542 P 19951103 US AE APPLICATION DATA (PATENT)
(APPL. DATA (PATENT))
US 552543 A 19951103
US 5867542 P 19951103 US AS02 ASSIGNMENT OF ASSIGNOR'S INTEREST
FUJUTSU LIMITED 1015 KAMIKODANAKA, NAKAHARA-KU, KAWASAKI-SHI KANAGAWA, JAPAN ; IWAMATSU, TAKANORI : 19950821; KIYANAGI, HIROYUKI : 19950818
US 5867542 P 19990202 US A PATENT